REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed July 22, 2003.

Currently, claims 1-6, 8 - 26 are pending. Applicants respectfully request reconsideration of claims 1-6, 8 - 26.

I. Summary of the Examiner's Objections

Claims 1-6, 8-11 and 19-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Chauhan (U.S. Patent No. 6,115,752).

Claims 1-6, 8-11 and 19-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Jindal et al. (U.S. Patent No. 6,324,580).

Claims 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Masuda et al. (U.S. Patent No. 6,201,810).

Claims 7 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauhan, or alternatively Jindal, in view of Masuda.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda, in view of Chauhan, or alternatively in view of Jindal.

II. Summary of the Amendments

Applicants have amended claims 1, 8, 11, 15, 17, 19, and 23, and cancelled claim 7.

II. Remarks

Claims 1 - 2

It is respectfully submitted claim 1 is not anticipated by Chauhan (U.S. Patent No. 6,115,752) nor Jindal et al. (U.S. Patent No. 6,324,580).

Claim 1 has been amended to include substantially the limitations of claim 7. Claim 1 now calls for:

the switch including a plurality of ports and respective processing circuitry affiliated with each respective port, the method comprising:

...

for port each, dynamically load balancing amongst the paths by the switch using said respective processing circuitry affiliated with each respective port on at least each request

The Examiner admitted that with respect to claim 7, Chauhan and Jindal "...fail to disclose that the switch includes a plurality of ports and wherein load balancing is performed by respective circuitry affiliated with each respective port."

Claim 7 was rejected as obvious over of Chauhan or Jindal, in view of Masuda. However, it is respectfully submitted that the combination of the above references would not lead one of average skill in the art to the method now defined in claim 1. In particular, one of average skill would not be led to combine the references in the manner suggested by the Examiner, nor would such combination result in the claimed invention.

Chauhan discloses a method for selecting mirrored sites using a round trip time for a name query or an echo packet (Col. 7, lines 24 – 65). The reference does not mention anything about the particular hardware used to connect or route data between the name servers or the mirrored servers. The only mention of particular hardware comes with respect of Figure 1 in the description of prior art which mentions gateways and routers.

Jindal likewise discloses only a method for directing a client to a replicated service, which *may* be performed using the response time for a request submitted to a server or service instance (Col. 6, lines 4 – 19). However, this is dependent on whether the particular policy of selected based on this criterion is in place (see Col. 6, lines 34 – 36). Again, no mechanism for routing traffic via a hardware mechanism is provided.

Masuda discloses a routing control system which, while including a plurality of ports, does not disclose "processing circuitry affiliated with each respective port". Indeed, in Masuda, the path candidate selection unit 11 is described in functional terms only, and the methods by which the unit selects amongst paths for routing information in the unit are discussed. The methods are not performed "dynamically".

Hence, as understood, the Examiner's conclusion of obviousness is based on the assertion that one of average skill seeking to implement the teachings of Chauhan and Jindal would be led to use the "circuitry affiliated with each respective port" taught by Masuda. (Office Action, Page 11, second full paragraph).

The Examiner points to the teachings of Masuda as enabling "a system for selecting between paths when connecting an initiator to a target device, wherein the switch used to connect the devices has multiple ports, each port connecting to a different member of the target device (Fig 1, col. 5, lines 25 – 35 and 51 – 54)". The Examiner concludes that "... it would have been obvious to a person having ordinary skill in the art to include the multiple ports taught by Masuda in either one of the systems taught by Chauhan or Jindahl, to provide for faster path selection."

However, nothing in Masuda, Chauhan nor Jindal leads one of average skill to combine the methods of Chauahn or Jindal with the structure of Masuda, or vice versa. Chauahn and Jindal deal with replicated services routing and mirrored site routing at a process level only, while Masuda deals with routing in an ATM network. Routing considerations in each respective case are not similar. Hence, one of average skill would not be led by the respective teachings of Masuda, Chauhan nor Jindal to any combination of the references.

Nevertheless, even were the references combined, the resulting combination would not lead one of average skill to the invention as now defined in claim 1.

In particular, there is no teaching of "respective processing circuitry affiliated with each respective port ... and ... for port each, dynamically load balancing amongst the paths by the switch using said respective processing circuitry affiliated with each respective port on at least each request...." as now defined in claim 1. Masuda does not teach processing circuitry associated with each port, only a "path candidate selection unit having a routing table with connection information. Processing is not performed by circuitry associated with each port.

Hence, in order to reach a construction of the device of the present invention, one of average skill would have to modify Masuda to include processing circuitry associated with each port, use the methods of the Chauahn and Jindal references, and then choose to use the port processing circuitry perform that functions described in Chauahn and Jindal to implement the load balancing functions.

It is respectfully submitted that one of average skill would not be led by these references to any such construction, and that the mere fact that three separate and independent jumps are required to reach this construction requires a conclusion that the invention as defined in claim 1 is not obvious.

It is respectfully submitted that claims 2 and 5 depending from claim 1 and including all the limitations of claim 1 are likewise not obvious for the reasons set forth above.

Claim 8

Claim 8 includes limitations similar to claim 1. In particular, claim 8 requires:

> .... a plurality of ports and respective processing circuitry affiliated with each respective port, the method comprising:
>
> passing a request received by the switch from the initiator to the storage device along the path with the shortest average response time using said affiliated processing circuitry.

For the reasons set forth above with respect to claim 1, it is respectfully submitted that claim 8 is not obvious nor anticipated by Masuda, Chauhan nor Jindal. Reconsideration of claim 8 is therefore respectfully requested.

Claim 9-10

Claim 9 includes limitations similar to claim 1. In particular, claim 9 requires:

> ....the switch including a plurality of ports and respective processing circuitry affiliated with each respective port, ...
>
> passing a request received by the switch from the initiator to the member with the shortest average response time using said affiliated processing circuitry.

For the reasons set forth above with respect to claim 1, it is respectfully submitted that claim 9, and claim 10 dependent therefrom, is not obvious nor anticipated by Masuda, Chauhan nor Jindal. Reconsideration of claims 9 and 10 is therefore respectfully requested.

Claims 11- 14

Claim 11 includes limitations similar to claim 1. In particular, claim 11 requires:

> A method for use in a storage network including a switch, the switch including a plurality of ports and respective processing circuitry affiliated with each respective port ...the method comprising:
> ...
> passing a first request received by the switch from the initiator to the physical storage device along the path to the physical storage device with the shortest average response time using said affiliated processing circuitry;
> passing a second request received by the switch from the initiator to the member of the mirrored target with the shortest average response time using said affiliated processing circuitry.

For the reasons set forth above with respect to claim 1, it is respectfully submitted that claim 11, and claims 12-14 dependent there from, is not obvious nor anticipated by Masuda, Chauhan nor Jindal. Reconsideration of claims 11 and 12-14 is therefore respectfully requested.

Claim 15 – 16

Claim 15 includes limitations similar to claim 1. In particular, claim 15 requires:

> .... load balancing circuitry associated with each port determining a respective average response time for a path and
> passing a request received by the switch from the initiator to a storage device along the path with the shortest average response time affiliated with each of the ports using said circuitry.

For the reasons set forth above with respect to claim 1, it is respectfully submitted that claim 15, and claim 16 dependent therefrom, is not obvious nor anticipated by Masuda, Chauhan nor Jindal. Reconsideration of claims 15 and 16 is therefore respectfully requested.

Claim 17- 18

Claim 17 includes limitations similar to claim 1. In particular, claim 17 requires:

a plurality of ports, at least one of the plurality of paths passing through at least one of the plurality of ports;

means for load balancing amongst the paths using processing circuitry associated with each of said ports.

Moreover, claim 17 includes a means plus function limitation and must be construed in light of the specification. In Re *Donaldson*, 16 F.3d 1189, 1193 (CAFC 1994), *en banc*, the Court stated:

> [t]he plain and unambiguous meaning of paragraph six is that one construing means-plus-function language in a claim must look to the specification and interpret that language in light of the corresponding structure, material, or acts described therein, and equivalents thereof, to the extent that the specification provides such disclosure. Paragraph six does not state or even suggest that the PTO is exempt from this mandate... *Id.* at 1193.

Under *Donaldson*,

> the "broadest reasonable interpretation" that an examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination. *Id.* at 1194-1195.

The Examiner has not pointed to the structural equivalent of any "means" as defined in claim 15 in the prior art.

For this reason, and for the reasons set forth above with respect to claim 1, it is respectfully submitted that claim 17, and claim 18 dependent therefrom, is not obvious nor anticipated by Masuda, Chauhan nor Jindal. Reconsideration of claims 17 and 18 is therefore respectfully requested.

Claim 19 – 22

Claim 19 includes limitations similar to claim 1. In particular, claim 19 requires:

a plurality of paths from the initiator to the target via at least one port the switch;

wherein the switch includes statistical information regarding the response time for each path; and

wherein the switch is designed to forward a request from the initiator to the target along the path with the shortest response time using processing circuitry affiliated with each of the ports.

For the reasons set forth above with respect to claim 1, it is respectfully submitted that claim 19, and claims 20-22 dependent therefrom, is not obvious nor anticipated by Masuda, Chauhan nor Jindal. Reconsideration of claims 19 and 20-22 is therefore respectfully requested.

Claims 23 - 26

Claim 23 includes limitations similar to claim 1. In particular, claim 23 requires:

> a plurality of paths from the initiator to the target via at least one port the switch;
> wherein the switch includes statistical information regarding the response time for each path; and
> wherein the switch is designed to forward a request from the initiator to the target along the path with the shortest response time using processing circuitry affiliated with each of the ports.

For the reasons set forth above with respect to claim 1, it is respectfully submitted that claim 23, and claims 24-26 dependent therefrom, is not obvious nor anticipated by Masuda, Chauhan nor Jindal. Reconsideration of claims 23 and 24-26 is therefore respectfully requested.

Based on the above amendments and these remarks, reconsideration of claims 1-6 and 8 – 26 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, December 19, 2003.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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By: _____
Larry E. Vierra
Reg. No. 33,809

VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 Market Street, Suite 540
San Francisco, California 94105-4206
Telephone: (415) 369-9660
Facsimile: (415) 369-9665